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CONTROLLED LIMITER IN THE SYNCHRONOUS DETECTION CIRCUIT

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Abstract. This variant of construction of the electrical circuit is aimed at reducing the effects of impulse noise. The measuring channels of the primary transducers are subject to interference of various types. In the case of a small ratio between a useful signal and noise level, synchronous detection is used. Impulse noise leaves a big mark even after using synchronous detection. To improve the performance of such measuring devices, it is proposed to use a controlled amplitude limiter at the input. Comparative analysis of solutions with controlled limiters is carried out in the article and conditions for its optimal operation are determined.

Keywords: synchronous detection, controlled limiter.

Introduction

Significant improvement of the quality control in modern manufacturing processes can be achieved on the basis of information on environmental parameters such as concentration, electrokinetic characteristics, etc. Most of the informative signals from the detectors of these parameters have a small amount comparable to the magnitude of the noise specific to the detector, or noise of industrial and natural origin (Titov 2009).

Statement of the problem and the object of study

One of the possible ways to improve the signal/noise ratio in such cases is the use of sensors with the modulated signal, and the selection of informative component by a synchronous detection. Primary transducers in industrial environments are affected by impulse noise of industrial origin. These disturbances have a broad spectrum, the amplitude of harmonics falling within the band of the signal, commensurable with the amplitude of an informative parameter that greatly affects the stability of the measuring instrument.

The level limiter that is known in measuring technique with the limits corresponding to the maximum value of the useful signal does not provide effective suppression of impulse noise in case when the signal is much less than the maximum. To improve the level of protection of informative signal against impulse noise structural diagram of a synchronous detector with a controllable limitation (CL) was developed.

To increase the efficiency of noise reduction impact on the output of the synchronous detector (SD) that was implemented on 2 multiplier and low pass filter (LPF) 3, limiter 1 with adjustable limit level was set. Setting the limits is carried out by normalizing amplifier 6 on the output (Fig. 1).

If there is a prior information about the low change rate of information parameter (which is often the case when measuring the electrical characteristics of the weak signals in chemical engineering processes), it may increase the

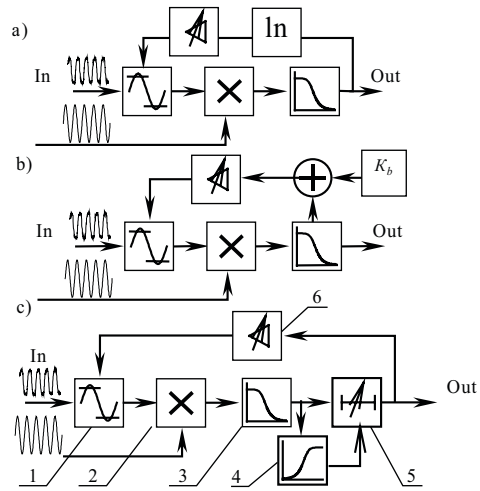

Fig. 1. Block diagrams of controlled limiter using: *a* – logarithmic amplifier: *b* – constant displacement; *c* – sample-and-hold device; 1 – input voltage protection; 2 – electronic multiplier; 3 – low pass filter (LPF); 4 – high pass filter (HPF); 5 – sample-and-hold device; 6 – controlled limiter.

stability of operation of the device due to the "blocking" the measuring path for the duration of impulse noise. This can be realized by noise detector that is provided on the HP filter (HPF) 4, and changes of the overwriting time of the output signal of sample-and-hold device (SHD) 5.

The structure of the measuring system (Fig. 1) has a number of settings (headroom level and time of the overwrite limitations), which significantly affects the effectiveness of the schematic design. Finding the optimal parameters using theoretical solutions is complicated by significant non-linearity associated with the presence of the multiplier, limiter and variable delay of sample-and-hold device (SHD).

To assess the effectiveness of application and determine the influence of the main structure of the settings controlled limiter (CL) a numerical simulation using the spectral analysis in an integrated environment MATLAB using Simulink applications was carried out. The noise signal has been selected as trapezoidal.

The calculation was performed for a reference signal with different characteristics, with varying parameters and noise at various levels of limitations. In the simulation, there were dynamic, static and integral quadratic errors.

In the simulation it was assumed that the useful signal frequency is equal to 17 rad/s (Hryniuk *et al*. 1998; Orobei *et al*. 2005). Additionally, a useful signal was superimposed with sinusoidal disturbance with a frequency of 50 Hz, noise components and random pulse disturbance with fixed parameters (period of 121.3 s, duration 1% of the period and amplitude of 50 times greater than the amplitude of the desired signal). The time constant of the filter at the output of the multiplier value was 10 and the ratio of the cut-off frequency w to the frequency of the useful signal w_S: $w/w_S = 0.0059$.

The simulation results exposed that usage of the controlled limiter in the structure of schematic components significantly reduces impulse noise at the converter output (Fig. 2).

Integral error and maximum dynamic deflection with the appearance of noise can be reduced by one to several tens. The coefficient K_b, which determines the headroom limitations, has the optimal value of the minimum quadratic integral errors, the maximum dynamic deflection or other criteria. For measuring circuit experimental structures optimum value K_b at the minimum integral square error or maximum dynamic deflection ranged from 1.5 to 4.5.

Moreover, for the same structure K_b optimal values for each of the different criteria differ. It should be noted that the approximation coefficient that determines the limitations level CL to one leads to the emergence of a large static error,

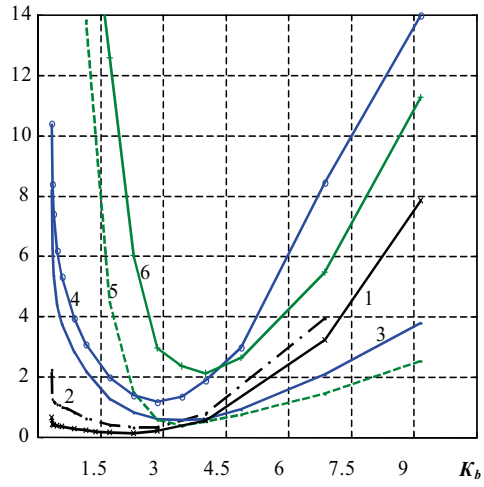

Fig. 2. The dependence of integral square error of K_b for different structure variants: 1 – CL with SD, SHD, and in the absence of HPF at the input; 2 – CL with SD, SHD in the absence of HPF at the input; 3 – CL with SD, SHD and HPF on the input with $w/w_S = 15.3$; 4 – CL with SD and in the presence of HPF on the input with $w / w_S = 15.3$; 5 – CL with SD and SHD and HPF on the input with $w/w_S = 29.4$; 6 – CL with SD and HPF on the input with $w/w_S = 29.4$.

which is especially evident in the presence of total signal noise. Introduction of SHD in the measuring circuit also improves its work; it reduces the maximum dynamic error. Device inertia is increased due SHD, it essentially occurs only at the moment of switching on the transmitter.

SD with CL in feedback are applicable only for sensors with a low rate of change in the information signal. The limiting level is selected basing on the maximum rate of increase of informative signal. When using schematic with a delay of informative signal for one clock cycle, the rise time to level limitations shall not exceed a period considering the inertia of the filter. This type of the schematic has been used in electrokinetic transducer.

The offered system solutions have certain disadvantages associated with the fact that the converter slowly passes zero point of the signal. To avoid this lack of amplifier, which determines the level of limitations bias was introduced. Reduction of the duration of the transitional process when installing is realized by limiting the maximum level when power is on.

For devices with a wide range of variation of the parameter information in the implementation of the proposed structure as the feedback unit it is more efficient to use the amplifier with logarithmic characteristic.

In the synchronous detector input signal is multiplied by an independent value from it periodically called function or switching vector. The spectrum of SD output is concentrated in the DC and harmonics of the switching

frequency, so the output value is a slowly varying function of the input signal. This property of the spectrum led to a number of specific features of the SD.

The primary converters to slow changes in the output signal superimposed internal interference, zero drift, switching phenomena, noises, etc. To isolate the desired signal on the background of periodical and non-interference must have a strictly sinusoidal function switching and low-pass filter or integrator. Represent the input signal $e_{IN}(t)$ and the switching function $Y(t)$ as:

$$e_{IN}(t) = \sum_{n=1}^{\infty} E_n \cos\left(n\omega t + \phi_n\right), \quad (1)$$

$$Y(t) = Y_0 \cos\left(\omega t\right). \quad (2)$$

Then, after multiplying obtain

$$i\left(t\right) = \frac{Y_0}{2} \sum_{n=1}^{\infty} E_n \left\{\cos\left[n\omega t + \phi_n\right]\cos\left(\omega t_n\right)\right\}. \quad (3)$$

If the oscillation to apply a low pass filter with a transmission coefficient

$$K\left(j\omega\right) = \frac{1}{1 + j\omega T}.$$

we get the expression of the form:

$$i\left(t\right) = \frac{Y_0}{2} \sum_{n=1}^{\infty} E_n \left\{\cos\left[\left(n-1\right)\omega t + \phi_n\right] + \right.$$
$$\left. + \cos\left(\left(n+1\right)\omega t + \phi_n\right) \frac{1}{\sqrt{1 + \left(n-1\right)^2 \omega^2 T^2}}\right\} \quad (4)$$

When $\omega T >> 1$ variable components with frequencies w, 2w, 3w ... can be significantly reduced, then

$$i'(t) = \frac{E_1 Y_0 \cos\left(\phi_1\right)}{2}. \quad (5)$$

Thus, the presence of periodic noise SD switching sine function allows to select the desired signal with very small amplitude, if the condition $\omega T >> 1$ is satisfied for the lowest noise frequency. However, this well-known conclusion applies to the idealized detector. In real SD selectivity deteriorates due to switching from the sinusoidal function differences. All this causes the relevance of the study of the causes and factors, which could affect the characteristics, improvement and development methods of SD.

Sufficiently small and stable frequency of the input signal and, consequently, the possibility of fine tuning the position reference information allows relatively ignored and the error angle signal simplify calculation. SD for the primary device is implemented using a linear multiplying circuit that allows varying the reference waveform. The simplest in terms of the analysis, but the most difficult to implement the reference waveform is a sine wave. The conductivity of the SD circuit is as follows:

$$Y_1\left(t\right) = Y_0 \cos\left(\omega t\right). \quad (6)$$

The output current at input signal in the absence of changes in the envelope can be found from the relation

$$i_0\left(t\right) = \frac{E_1 Y_0}{2}, \quad (7)$$

therefore DC component is proportional to the amplitude of the fundamental harmonic.

Also for comparison to the harmonic circuitry the relay switching SD can be realized for triangular and trapezoidal shapes of input signal.

The function of the relay switching SD described by the relation

$$Y\left(t\right) = Y_0 \operatorname{sign}\left[\cos\left(\omega t\right)\right]. \quad (8)$$

When applying a sinusoidal signal to a synchronous detector with relay conductivity change

$$\operatorname{sign}\left(\cos\omega t\right) = \frac{4}{\pi} \sum_{p=1}^{\infty} \frac{\cos\left[\left(2p-1\right)\omega t\right]}{2p-1}, \quad (9)$$

output current (considering the expansion switching function in a Fourier series) can be written as:

$$i\left(t\right) = E_n Y_0 \sum_{n=1}^{\infty} \frac{\cos\left[\left(2n-1\right)\omega t\right] + \cos\left[\left(2n+1\right)\omega t\right]}{0.5\left(2p-1\right)\pi}. \quad (10)$$

After the necessary filtering is only the constant component

$$i_0\left(t\right) = \frac{2E_n Y_0}{\pi}. \quad (11)$$

For non-sinusoidal input DC output after filtration contains an infinite number of terms. Relay output signal SD in contrast to a harmonic depends not only on the amplitude and phase of the first harmonic, but also from the higher odd harmonics. Given that the amplitude of the higher harmonics in real systems rapidly decreases with an increase of their number, it can be concluded that the largest effect on the result of having the third harmonic.

Reduce the impact on the results of demodulation of higher harmonics of the reference and input signal, and harmonics of low-frequency short-pulse noise for the proposed converter can be several ways. In the following possible options for pulse shapes: trapezoidal and triangular. And a ratio can be selected on the criterion of maximum power of the fundamental harmonic relationship to full power.

Numerical analysis of SD with CL was made with the spectral method. Efficiency was evaluated by changing

the ratio of useful energy at the output of the synchronous detector (constant component of the first harmonic) to the energy of the remaining components. In general, the signal / noise ratio at the output of SD is expressed as:

$$RSN = \frac{CS_1 CD_1}{2(PN + PS)}\left(1 - \frac{Lw}{2\pi}\right), \qquad (12)$$

where

$$PN = \sum_{m=1}^{2}\sum_{i=1}^{\infty}\sum_{n=1}^{\infty}\left(\frac{CN_n CD_i}{2\sqrt{1+\left(\omega i + (-1)^m wn\right)^2 T_f^2}}\right)^2, \qquad (13)$$

$$PS = \sum_{m=1}^{2}\sum_{i=1}^{\infty}\sum_{k=2}^{\infty}\left(\frac{CS_k CD_i}{2\sqrt{1+\left(\omega\left(k + (-1)^m i\right)\right)^2 T_f^2}}\right)^2, \qquad (14)$$

here: PN – power components at the output SD, caused by the presence of noise; PS – power components at the output SD caused by the presence in the informative signal of higher order harmonics; L – length of noise; w – frequency noise; w – the frequency of measurement and the reference signal; CS_k – coefficients of signal harmonics; CN_n – noise ratios of harmonics; CD_i – coefficients of the harmonics of the reference signal; T_f – time constant of the low-pass filter at the output of SD.

Then limiter efficiency can be defined as:

$$RSN_1 \Big/ RSN_0 = \frac{PN_0 + PS}{PN_1 + PS}, \qquad (15)$$

here: RSN_1, PN_1 – signal/noise ratio and power at the output SD, caused by the presence of interference with CL; RSN_0, PN_0 – S/N ratio without the use of CL.

Maximum efficiency is observed when CL harmonic information and the reference signal, as this $PS = 0$. Let us assume that an obstacle has trapezoidal shape, which is due to its limitation level chip-level power. In assessing the effectiveness of CL the following pattern was received; the less informative value of the signal amplitude with respect to the power level, the more effective is use of CL, i.e. the most justified use of such devices with weaker signals.

Conclusions

1. The proposed and investigated circuit solution with fixing the level of the limit for some time with the detection of impulse noise makes it possible to increase the signal-to-noise ratio in the measuring channel.
2. The proposed method of suppressing noise components can be used in digital measuring devices. The control and optimization algorithm is easily implemented on the microcontroller, and the constraint can be built using a digital-to-analog converter.

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VALDOMAS RIBOTUVAS SINCHRONINIO DETEKTORIAUS ĮTAISE

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Santrauka

Matavimo grandinėse pirminiai keitikliai yra veikiami įvairaus pobūdžio trikdžių. Dėl žemo signalo / trikdžių lygių santykio panaudotas sinchroninis detektorius. Impulsiniai trikdžiai palieka žymes sinchroninio detektoriaus išėjimo signale. Tyrimo tikslas yra patobulinti įtaiso elektrinę grandinę siekiant sumažinti impulsinių trikdžių įtaką. Tuo tikslu pasiūlyta įtaiso įėjime panaudoti valdomą amplitudės ribotuvą ir atlikta jo valdymo būdų lyginamoji analizė, apibrėžtos optimalios veikimo sąlygos.

Reikšminiai žodžiai: sinchroninis detektorius, valdomas ribotuvas.